Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method of designing an integrated circuit comprising:
   a. generating a plurality of sequences of basic Boolean elements respectively defined by a plurality of truth tables;
   b. generating a respective plurality of substitute circuits not definable by a sequence of basic Boolean elements, including a first substitute circuit, wherein the sequence of basic Boolean elements and the respective substitute circuit are defined by a same truth table;
   c. storing the plurality of sequences of basic Boolean elements in a library;
   d. storing the plurality of substitute circuits in the library in a relationship corresponding to their respective sequence of basic Boolean elements;
   e. programming a processing path within the integrated circuit according to ~~a~~ the first substitute circuit comprising substitute inputs and a substitute output, wherein ~~a~~ the truth table representing the first substitute circuit is identical to ~~a~~ the truth table representing a first sequence of basic Boolean elements representing ~~a~~ the processing path, and wherein the first substitute circuit is not definable by a sequence of basic Boolean ~~circuits~~ elements;
   f. reducing the first sequence of basic Boolean elements into at least one intermediate equivalent circuit; and
   g. generating the first substitute circuit.

2. (canceled).

3. (currently amended) The method according to claim [[2]] 1 further comprising receiving the first sequence of basic Boolean elements.

4. (original) The method according to claim 1 wherein the processing path further comprises a flip flop at a processing path input.

5. (canceled).

6. (currently amended) The method according to claim [[2]] 1 wherein the integrated circuit is a MOS circuit.

7. (original) The method according to claim 3 wherein the first sequence of basic Boolean elements is less than or equal to twenty Boolean operators.

8. (original) The method according to claim 3 wherein the first sequence of basic Boolean elements comprises a logical sequence greater than twenty Boolean elements.

9. (currently amended) The method according to claim 3 wherein ~~the step of~~ receiving the first sequence of basic Boolean elements precedes ~~the step of~~ generating a respective plurality of substitute circuits not definable by a sequence of basic Boolean elements, including a first substitute circuit.

10. (canceled).

11. (currently amended) The method according to claim ~~10~~ 1 further comprising ~~the steps~~:
~~c.~~ a. receiving a the first sequence of basic Boolean elements; and
~~f.~~ b. searching the library for the first substitute circuit.

12. (currently amended) The method according to claim 11 further comprising ~~the steps~~:
a. failing to locate the first sequence of basic Boolean elements within the library;
b. generating the first substitute circuit; and
c. adding the first substitute circuit to the library.

13. (currently amended) The method according to claim 11 wherein ~~the step of~~ receiving the first sequence of basic Boolean elements is followed by ~~the steps~~:
a. locating the first sequence of basic Boolean elements within the library; and
b. locating the first substitute circuit within the library corresponding to the first sequence of basic Boolean elements.

14. (currently amended) The method according to claim ~~10~~ 1 wherein the library ~~comprises~~ is stored within a digital memory.

15. (currently amended) The method according to claim 11 ~~comprising a search engine for searching~~ wherein the library is searched for the first sequence of basic Boolean elements utilizing a search engine.

16. (currently amended) An apparatus for reducing a throughput time of a processing path of basic logic elements within an integrated circuit, the apparatus comprising:

a. a sequence generator for generating a plurality of sequences of Boolean elements, wherein the circuit generation module is configured to generate a complimentary substitute circuit for each sequence of Boolean elements generated;

b. a library for storing the plurality of sequences of Boolean elements such that each Boolean element is stored in a correlation to its complimentary substitute circuit;

c. a search module for searching the library for a first sequence of Boolean elements;

d. a retrieval module for retrieving a substitute circuit from the library;

e. a programming module for programming a first substitute circuit into the processing path of the integrated circuit, wherein the first substitute circuit is not defined by a sequence of ~~basic~~ Boolean ~~circuits~~ elements, and wherein the first substitute circuit is defined by ~~a~~ the truth table identical to a truth table defining ~~a~~ the processing path comprised of ~~basic~~ the sequence of Boolean ~~circuits~~ elements; and

f. a circuit generation module configured to analyze the first sequence of Boolean elements, reduce the first sequence of Boolean elements into an intermediate circuit sequence and then generate the complimentary substitute circuit.

17. (original) The apparatus according to claim 16 wherein the processing path comprises an input flip flop.

18. (original) The apparatus according to claim 16 wherein the integrated circuit is an MOS circuit.

19. (canceled).

20. (canceled).

21. (canceled).

22. (currently amended) The apparatus according to claim ~~21~~ 16 wherein the library is stored on a digital medium.

23. (currently amended) A method of programming a processing path comprising an input flip flop in a MOS integrated circuit comprises:

a. generating a plurality of sequences of basic Boolean elements respectively defined by a plurality of truth tables;

b. generating a respective plurality of substitute circuits not definable by a sequence of basic Boolean elements, including a first substitute circuit, wherein the sequence of basic Boolean elements and the respective substitute circuit are defined by a same truth table;

c. storing the plurality of sequences of basic Boolean elements in a library;

d. storing the plurality of substitute circuits in the library in a relationship corresponding to their respective sequence of basic Boolean elements;

~~a.~~ e. receiving a first sequence of basic Boolean elements;

~~b.~~ f. reducing the first sequence of basic Boolean elements to an equivalent sequence of elements;

~~c.~~ g. generating a first substitute circuit from the equivalent sequence of elements; and

~~d.~~ h. programming a the processing path in the MOS integrated circuit according to the first substitute circuit, wherein the substitute circuit is not definable by a sequence of basic Boolean elements, and wherein the first substitute circuit is generated to define a first truth table that also defines the first sequence of Boolean elements.